Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.082”**

**PAD FUNCTION:**

1. **V+**
2. **NC**
3. **NC**
4. **IN 16**
5. **IN 15**
6. **IN 14**
7. **IN 13**
8. **IN 12**
9. **IN 11**
10. **IN 10**
11. **IN 9**
12. **GND**
13. **NC**
14. **A3**
15. **A2**
16. **A1**
17. **A0**
18. **EN**
19. **IN 1**
20. **IN 2**
21. **IN 3**
22. **IN 4**
23. **IN 5**
24. **IN 6**
25. **IN 7**
26. **IN 8**
27. **V-**
28. **OUT**

**19**

**20**

**21**

**22**

**23**

**24**

**25**

**26**

**18 17 16 15 14 12**

**27 28 1 2**

**11**

**10**

**9**

**8**

**7**

**6**

**5**

**4**

**.129”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: -V or FLOAT**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .082” X .129” DATE: 8/25/21**

**MFG: HARRIS/INTERSIL THICKNESS .014” P/N: HIO-506**

**DG 10.1.2**

#### Rev B, 7/1